Having thus described the preferred embodiments, the invention is now claimed to be:

1. A digital signal processing apparatus comprising:

a means **(12)** for converting a received video signal into a stream of digital numbers arranged in a sequence of digitized video frames, neighboring frames being separated by a synchronization signal;

a means **(20)** for compressing the digitized frames;

a means **(30)** for monitoring the synchronization signals; and

a means **(32)** for generating a synchronization signal in accordance with the monitored synchronization signals for clocking the digitized frames compressing means.

2. The apparatus as set forth in claim 1 wherein at least one synchronization signal is absent.

3. The apparatus as set forth in claim 2 wherein the monitoring means **(30)** detects an absence of the at least one synchronization signal.

4. The apparatus as set forth in claim 3 wherein the generating means **(32)** generates a replacement synchronization signal for the at least one absent synchronization signal.

5. The apparatus as set forth in claim 4 further including:

a means **(18)** for storing at least one digitized frame.

6. The apparatus as set forth in claim 4 wherein the means **(12)** for converting the received analog signal into the stream of digital numbers includes at least one analog-to-digital converter.

7. The apparatus as set forth in claim 4 wherein the means **(32)** for generating the replacement synchronization signal includes:

a fixed clock **(40)** for generating the replacement synchronization signals for the sequence of digitized frames at a fixed rate.

8. The apparatus as set forth in claim 7 further including:

a means **(18)** for buffering digitized frames during monitoring for the absence of synchronization signals, and generating of the replacement synchronization signal and inserting synchronization signals during the absence of incoming synchronization signals.

9. The apparatus as set forth in claim 4 further including:

a means **(42)** for determining a clock rate of the synchronization signals in one of the video signals and the sequence of digitized frames.

10. The apparatus as set forth in claim 9 wherein the means **(32)** for generating the replacement synchronization signal includes:

a means **(44)** for inserting the replacement synchronization signal into the sequence of digitized frames at the determined clock rate of the synchronization signals.

11. The apparatus as set forth in claim 10 further including:

a means **(18)** for storing at least two digitized frames to delay for the generation of replacement synchronization signals.

12. The apparatus as set forth in claim 4 further including:

a means **(18)** for storing a plurality of the digital frames; and,

a means **(42)** for averaging a clock rate of the synchronization pulses of the frames in the storing means and controlling the generating means to generate the replacement synchronization signals locked to the average clock rate.

13. The apparatus as set forth in claim 4 wherein the compressing means **(20)** is clocked by stable synchronization pulses when present and by pulses from the generating means in the absence of sensed synchronization pulses.

14. A method of processing digital signal comprising:

converting received video signals into a sequence of digital values, the video signals and the digital values sequence including synchronization signals that denote at least an interface between adjacent frames;

monitoring the synchronization signals of one of the video signals and the digital values sequence;

generating replacement synchronization signals; and

compressing the digitized frames in accordance with the generated replacement synchronization signals.

15. The method as set forth in claim 14 wherein the monitoring step includes:

monitoring for absent synchronization signals.

16. The method as set forth in claim 14 wherein the generating step includes:

generating a replacement synchronization signal at least for each absent synchronization signal.

17. The method as set forth in claim 16, further including:

inserting the replacement synchronization signals into the sequence of digitized frames at a fixed clock rate.

18. The method as set forth in claim 16, further including:

determining a frequency of the synchronization signals, the replacement synchronization signals being generated at the determined frequency.

19. The method as set forth in claim 18, further including:

in response to detecting absent synchronization signals before the clock rate of the synchronization signals is determined, generating the replacement synchronization signals at a preselected fixed clock rate.

20. The method as set forth in claim 14, further including:

monitoring a frequency of the synchronization signals; and

averaging the frequency over a plurality of the synchronization signals to determine an actual clock rate of the synchronization signals.

21. The method as set forth in claim 20, further including:

buffering a plurality of the digitized frames.

22. The method as set forth in claim 21, further including:

generating the replacement synchronization signals at the average frequency of the buffered digitized frames.

23. The method as set forth in claim 20 wherein the synchronization signal frequency is averaged for a preselected duration.

24. The method as set forth in claim 14 wherein the monitoring step includes:

monitoring for the synchronization signals in a time window based on a preselected nominal synchronization clock rate.

25. The method as set forth in claim 24 wherein the compressing step uses one of "MPEG" and "AMPEX DCT" compression.

26. The method as set forth in claim 14 further including:

clocking the compressing of the digitized frames with stable synchronization pulses;

monitoring for the absence of stable synchronization signals; and

in the absence of stable synchronization signals, inserting the replacement synchronization signals.

27. An audio/video digital imaging system comprising:

an analog-to-digital converter **(12)** which receives video signals and converts them into a sequence of digitized frames, adjacent pairs of frames being separated by a synchronization signal;

a sensing circuitry **(30)** which monitors for the synchronization signals;

a clock **(32)** which generates replacement synchronization signals in accordance with the monitored synchronization signals; and

a compression circuitry **(20)** which compresses the digitized frames at a clock rate set by the replacement synchronization signals.